Chapter 3

Diodes and Applications

3.1 Introduction [5], [6]

Diode is the most basic of semiconductor device. It should be noted that the term of diode refers to the basic p-n junction diode. All other diode types have other identifying names, such as zener diode, light-emitting diode and so on. A diode is a two-electrode (two-terminal) device that acts as a one-way conductor. When forward biased, the diode will conduct. When reverse biased, diode conduction will drop to nearly zero. Here, a diode circuit is shown in Figure 3.1.

![Diode circuit symbol](image)

Figure 3.1 Diode circuit symbol [6]
3.2 Bias Connections [5]

**Forward-Bias connection:** A diode is forward-biased when a voltage source is connected as shown in Figure 3.2(a). The positive terminal of the source is connected to the anode through a resistor. The negative terminal of the source is connected to the cathode. The forward current \( I_F \) is from anode to cathode as indicated. The forward voltage drop \( V_F \) due to the barrier potential is from positive at the anode to negative at the cathode.

**Reverse-Bias Connection:** A diode is reverse-biased when a voltage source is connected as shown in Figure 3.2(b). The negative terminal of the source is connected to the anode side of the circuit, and the positive terminal is connected to the cathode side. The reverse current is extremely small and can be considered to be zero. Notice that the entire bias voltage \( V_{\text{BIAS}} \) appears across the diode.

![Diagram of Forward and Reverse Bias Connections](image-url)

Figure 3.2 Forward-bias and reverse-bias connections showing the diode symbol. [5]
3.3 Diode Circuit Analysis [5], [6]

Figure 3.2 shows a Diode circuit containing a voltage source and a resistor. Here, in order to analyze the current passing the diode (I_D) and the voltage across the diode (V_D), we can use 4 methods as mentioned below.

- Mathematical Model
- Ideal Diode Model
- Constant Voltage Drop (CVD) Model
- Complete Diode Model

![Diode circuit containing a voltage source and a resistor](image)

Figure 3.3 Diode circuit containing a voltage source and a resistor.

**Steps to analyze I_D and V_D in the diode circuit:**

1. Select a model for the diode.
2. Make a guess concerning the region of operation for the diode based on the circuit configuration.
3. Analyze the circuit using the model appropriate for the assumption in step 2.
4. Check the results to see if they are consistent with the assumptions.
3.3.1 Analysis Using the Mathematical Model

Example 1: Use Mathematical Model to analyze $I_D$ and $V_D$ from Figure 3.3.

- Apply KVL to the loop.
  
  $$-10 + 10^4 I_D + V_D = 0$$

  $$\therefore 10^4 I_D + V_D = 10 \quad (1)$$

- From the equation
  
  $$I_D = I_S \left( e^{\frac{V_D}{V_T}} - 1 \right) \quad (2)$$

- Substitute (2) in (1) with $I_S = 10^{-13}$ A, $V_T = 0.025$ V. (for Si diode @ room temperature)
  
  $$10^{-9} \left( e^{40V_D} - 1 \right) + V_D = 10 \quad (3)$$

- Solve (3) for $V_D$, then $V_D = 0.5742$ V and $I_D = 9.426 \times 10^{-4}$ A = 0.9426 mA

3.3.2 Analysis using Ideal Diode Model

The ideal model of a diode is the least accurate approximation and can be represented by a simple switch. When the diode is forward-biased, it ideally acts like a closed (on) switch, as shown in Figure 3.4(a). When the diode is reverse-biased, it ideally acts like an open (off) switch, as shown in part (b).

In Figure 3.5, the ideal V-I characteristic curve graphically depicts the ideal diode operation. The diode is assumed to have a zero voltage across it when forward-biased, as indicated by the portion of the curve on the positive vertical axis. Since the reverse current is neglected, its value is assumed to be zero, as indicated in Figure 3.5 by the portion of the curve on the negative horizontal axis.
Figure 3.4 The ideal model of a diode. [5]
(a) Equivalent circuit under forward bias (on or short circuit).
(b) Equivalent circuit under reverse bias (off or open circuit).
Therefore, using ideal diode model under this diode circuit condition, we can conclude that:

**For forward bias:** \( V_F = 0 \text{ V} \), and \( I_F = \frac{V_S}{R} \)

**For reverse bias:** \( I_R = 0 \text{ A} \), and \( V_R = -V_S \)
**Example 2:** Use ideal diode model to analyze $I_D$ and $V_D$ from Figure 3.3.

**Solution:** Consider from 4 steps to analyze $I_D$ and $V_D$ in the diode circuit:

1. Use the ideal diode model for this circuit condition (from Figure 3.3)

   ![Diagram 1](image1)

   (Figure 3.3)

2. Because the voltage source appears to be trying to forward bias the diode, we assume that the diode is on or acts like a short circuit, see Figure 3.6.

   ![Diagram 2](image2)

   Figure 3.6 For Example 2

3. Find $I_D$: $I_D = \frac{V_S}{R} = \frac{10 \, V}{10 \, k\Omega} = 1 \, mA$

4. The current $I_D > 0$, which is consistent with the assumption that the diode is on.
Example 3: Use ideal diode model to analyze $I_D$ and $V_D$ of both diodes from Figure 3.7.

![Figure 3.7 For Example 3](image)

Solution:

- Use the ideal diode model
- Make assumptions. Because we have 2 diodes in this circuit. Therefore we can assume 4 conditions, as mentioned in Table 1.

Table 1: 4 possible diode conditions for 2 diodes

<table>
<thead>
<tr>
<th>Possible Diode States</th>
<th>D1</th>
<th>D2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Off</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td>On</td>
<td>On</td>
<td>Off</td>
</tr>
</tbody>
</table>
**First try:** Both diodes are on. Under this assumption, the diode circuit from Figure 3.7 becomes

![Diode Circuit](image)

Figure 3.8 Diode circuit with both diodes assumed to be on.

- **Find** \( I_{D1} \) and \( I_{D2} \).

\[
I_{D2} = \frac{0 - (-10)}{5k} = 2\text{mA}
\]

\[
I_1 = \frac{15 - 0}{10k} = 1.5\text{mA}
\]

\[
I_1 = I_{D1} + I_{D2}
\]

\[
I_{D1} = I_1 - I_{D2} = 1.5 - 2 = -0.5\text{mA}
\]

- The result \( I_{D1} < 0 \) is inconsistent with our assumption that \( D_1 \) is on. Our assumption must be incorrect.
**Second try**: $D_1$ is off and $D_2$ is on. Under this assumption, the diode circuit from Figure 3.7 becomes

![Figure 3.9 Diode circuit with D1 “Off” and D2 “On”](image)

- Find $I_{D2}$ and $V_{D1}$.

![Figure 3.10 Diode circuit with D1 “Off” and D2 “On”](image)
\[ I_{D2} = \frac{15 - (-10)}{10k + 5k} = 1.67 \text{ mA} \]

\[-15 + (10k \times I_{D2}) + V_{D1} = 0\]

\[ V_{D1} = 15 - 16.7 = -1.67 \text{ V} \]

- Since \( I_{D2} > 0 \) (\( D_2 \) is on) and \( V_{D1} < 0 \) (\( D_1 \) is off or reverse biased), they are consistent with our assumptions.

- We can conclude that

\[ I_{D1} = 0 \text{ A}, \quad V_{D1} = -1.67 \text{ V}, \quad I_{D2} = 1.67 \text{ mA}, \quad V_{D2} = 0 \text{ V} \]

**Example 4:** Determine \( I_{D1}, I_{D2}, V_{D1} \) and \( V_{D2} \), using ideal diode model.

Figure 3.11 For Example 4
Solution:

Keep in mind that by using ideal diode model,

- For on condition: $V_D = 0 \text{ V}$ and $I_D > 0 \text{ A}$
- For off condition: $V_D < 0 \text{ V}$ and $I_D = 0 \text{ A}$

First try: Assume diode 1 is on, diode 2 is off. Under this assumption, the diode circuit from Figure 3.11 becomes

![Diode Circuit Diagram](image)

Figure 3.12 For Example 4

- Find $I_D$ and $V_D$ off both diodes.

**Loop 1:** $I_1 = \frac{-15 \text{ V}}{15 \Omega} = -1 \text{ A}$

**Loop 2:** $I_2 = 0 \text{ A}$

Here $I_{D1} = I_1 - I_2$, Therefore $I_{D1} = I_1 = -1 \text{ A}$ (X)

**Loop 2:** $-10 + V_{D2} + 10I_2 + 20 = 0$

$V_{D2} = -10 \text{ V} \quad \checkmark$
**Second try** : Assume both diodes are off. Under this assumption, the diode circuit from Figure 3.11 becomes

![Diode Circuit Diagram](image)

**Figure 3.13 For Example 4**

- Find $I_D$ and $V_D$ off both diodes.

**Loop 1** : $+15 + 15I_1 + V_{D1} = 0$

$I_1 = I_{D1} + I_{D2} = 0 + 0 = 0 \ A$

$\therefore V_{D1} = -15 \ V \ (\checkmark)$

**Loop 2** : $-10 + V_{D2} + 10I_2 + 20 - V_{D2} = 0$

$I_2 = I_{D2} = 0 \ A$

$\therefore V_{D2} = -25 \ V \ (\checkmark)$

$\therefore I_{D1} = 0 \ A, I_{D2} = 0 \ A, V_{D1} = -15 \ V \ and \ V_{D2} = -25 \ V$
3.3.3 Constant Voltage Drop (CVD) Model or Practical Diode Model

The Constant Voltage Drop (CVD) Model (or Practical Diode Model) includes the barrier potential. When the diode is forward-biased, it is equivalent to a closed switch in series with a small equivalent voltage source ($V_F$) equal to the barrier potential (0.7 V for Si diode, 0.3 V for Ge diode) with the positive side toward the anode, as indicated in Figure 3.14(a). This equivalent voltage source represents the barrier potential that must be exceeded by the bias voltage before the diode will conduct and is not an active source of voltage. When conducting, a voltage drop of 0.7 V appears across the Si diode or 0.3 V appears across the Ge diodes.

When the diode is reverse-biased, it is equivalent to an open switch just as in the ideal model, as shown in Figure 3.14(b). The barrier potential does not affect reverse bias.

![Practical diode model](image)

Figure 3.14 The constant voltage drop (CVD) model
(or practical diode model of a diode). [5]

The characteristic curve for the practical diode model is shown in Figure 3.15. Since the barrier potential is included, the diode is assumed to have a voltage across it when forward-biased, as indicated by the portion of the curve to the right of the origin.
Therefore, using CVD model under this diode circuit condition, we can conclude that;

**For forward bias:**

\[ V_F = 0.7 \text{ V (for Si diode)} \quad \text{and} \quad V_F = 0.3 \text{ V (for Ge diode)} \]

Here, applying Kirchoff’s voltage to find \( I_F \):

\[ V_S - V_F - V_{R_{\text{Limit}}} = 0 \]

And

\[ V_{R_{\text{Limit}}} = I_F \times R_{\text{Limit}} \]

Therefore,

\[ I_F = \frac{(V_S - V_F)}{R_{\text{Limit}}} \]

**For reverse bias:**

\[ I_R = 0 \text{ A}, \quad \text{and} \quad V_R = -V_S \]
Example 5: Use CVD model to analyze $I_D$ and $V_D$ from Figure 3.3.

Solution: Consider from 4 steps to analyze $I_D$ and $V_D$ in the diode circuit:

1. Use the CVD model for this circuit condition (from Figure 3.3)

(Figure 3.3)

2. Because the voltage source appears to be trying to forward bias the diode, we assume that the diode is on, and we can replace Si diode by $V_F = 0.7$ V, see Figure 3.16.

(Figure 3.16 For Example 5)
3. Find $I_D$:

\[
I_D = \frac{10 - 0.7}{10k} = 0.93 \text{ mA}
\]

4. The current $I_D > 0$, which is consistent with the assumption that the diode is on.

*** Here, comparison of Diode Circuit Analysis (from Example 1, 2, 5) Results

<table>
<thead>
<tr>
<th>Analysis Method</th>
<th>Diode Current</th>
<th>Diode Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mathematical model</td>
<td>0.942 mA</td>
<td>0.547 V</td>
</tr>
<tr>
<td>Ideal diode model</td>
<td>1.00 mA</td>
<td>0 V</td>
</tr>
<tr>
<td>Constant voltage drop model</td>
<td>0.93 mA</td>
<td>0.7 V</td>
</tr>
</tbody>
</table>

**Example 6**: Use CVD model to analyze $I_{D1}$, $I_{D2}$, $I_{D3}$, $V_{D1}$, $V_{D2}$, and $V_{D3}$.

Figure 3.17 For Example 6
Solution: Here, we assume $D_1 = \text{off}$, $D_2 = \text{on}$, $D_3 = \text{on}$.

![Figure 3.18 For Example 6](image)

\[
\therefore V_{D_3} = -10 \, V, \quad V_{D_2} = 0.7V, \quad V_{D_1} = 0.7V, \quad I_1 = 0 \, A
\]

KVL loop2: 
\[
-10 + 0.7 + 5I_2 + 0.7 + 2(I_2 - I_4) = 0
\]
\[
\therefore \quad I_4 = 3.5I_2 - 4.3 \quad (1)
\]

KVL loop3: 
\[
-2(I_2 - I_4) - 0.7 + 10I_4 - 5 = 0
\]
\[
\therefore \quad 12I_4 = 2I_2 + 5.7 \quad (2)
\]

From (1), (2) 
\[
I_2 = 1.4325 \, A, \quad I_4 = 0.714 \, A
\]
\[
I_3 = I_2 - I_4 = 0.719 \, A
\]
Example 7: Using CVD model, calculate $V_O$, $I_{D_1}$, $I_{D_2}$, and $I$ for the following conditions:

(a) $V_1 = V_2 = 0 \, V$

(b) $V_1 = 20 \, V$, $V_2 = 0 \, V$

Solution :

(a) When $V_1 = V_2 = 0 \, V$, we assume $D_1 = \text{on}$, $D_2 = \text{on}$, see Figure 3.20.

\[
10 = 5I + 0.7 + 5*\frac{I}{2} \\
I = 1.24 \, A \\
I_{D_1} = I_{D_2} = I/2 = 0.62 \, A \\
V_0 = 0.7 + 5*I_{D_1} \, (or \, I_{D_2}) = 3.8 \, V
\]
(b) When $V_1 = 20$ V, $V_2 = 0$ V, we assume $D_1 = \text{off}$, $D_2 = \text{on}$, see Figure 3.21.

$$I_{D_1} = 0 \text{ A}$$

$I = I_{D_2}$

$10 = 5I + 0.7 + 5I_{D_2}$

$I = 9.3 \text{ A} = I_{D_2}$

$V_0 = 0.7 + 5I_{D_2}$

$= 0.7 + 5 \times (9.3)$

$= 5.35 \text{ V}$
3.4 Homework 3

1. Using ideal diode model, calculate the voltage across each diode and the current flowing through each diode in Figure 3.22 (a), (b) and (c).

![Figure 3.22 For problem 1](image)

2. Using ideal diode model, calculate $I_{D1}$, $I_{D2}$ in the circuit for each case.

   (1) $V_{IN} = 0$ V
   
   (2) $V_{IN} = 10$ V
   
   (3) $V_{IN} = -10$ V
3. Assume D₁, D₂ and D₃ are Si diodes. Find I₁, I₂, I₃, V₁, V₂ and V₃ in the circuit of Figure 3.24, using the ideal diode model.
4. Assume $D_1$ and $D_2$ are Si diodes. Find $I_{D1}$, $I_{D2}$, $V_{D1}$, $V_{D2}$ and $V_O$ in the circuit of Figure 3.25, using the ideal diode model.

![Figure 3.25 For problem 4](image)

5. Assume $D_1$ and $D_2$ are Si diodes. Find $I_{D1}$, $I_{D2}$, $V_{D1}$, $V_{D2}$ and $I_O$ in the circuit of Figure 3.26, using the ideal diode model.

![Figure 3.26 For problem 5](image)
6. Using CVD model, assume $D_1$, $D_2$, $D_3$ are Si diodes. Calculate $V_{OUT}$ and the currents $I_{D1}$, $I_{D2}$, $I_{D3}$ and $I$ for the following input conditions:

(a) $V_1 = V_2 = 0$ V

(b) $V_1 = 5$ V, $V_2 = 2$ V

Figure 3.27 For problem 6
7. Let $V_{on}$ (or $V_F$) = 0.6 V. Determine $I_D$ and $V_D$ in the circuit for each condition, using the CVD model.

(a) $V_1 = 15$ V, $V_2 = 10$ V
(b) $V_1 = 10$ V, $V_2 = 15$ V

![Figure 3.28 For problem 7](image)

8. (a) Assume $D_1$ and $D_2$ are Si diode, Find $I$, $V_{OUT}$, $I_{D1}$ and $I_{D2}$ in the circuit, using the CVD model.

(b) Assume $D_1$ is Si diode but $D_2$ is Ge diode, Find $I$, $V_{OUT}$, $I_{D1}$ and $I_{D2}$ in the circuit, using CVD model.

![Figure 3.29 For problem 8](image)
9. Assume D₁, D₂ and D₃ are Si diodes. Find $I_{D1}$, $I_{D2}$, $I_{D3}$, $V_{D1}$, $V_{D2}$ and $V_{D3}$ in the circuit of Figure 3.30, using the CVD model.

Figure 3.30 For problem 9
10. Assume the diode shown here is Ge diode. Find $I_D$, $V_D$ and $I_X$ in the circuit of Figure 3.31, using the CVD model.

![Figure 3.31 For problem 10](image)

11. Find $I_{D1}$, $I_{D2}$, $V_{D1}$, $V_{D2}$ and $V_O$ in the circuit of Figure 3.32, using the CVD model. Assume $D_1$ is Si diode and $D_2$ is Ge diode.

![Figure 3.32 For problem 11](image)
3.5 DC Power Supplies [5], [6]

One of the most important applications of diodes is in the design of rectifier circuits. Almost all electronic circuits require a dc source of power. For portable low power systems, batteries may be used. However, most electronic equipment relies on a line-operated dc power supply.

As shown in Figure 3.33, the first block in a dc power supply is the power transformer. This block provides the appropriate sinusoidal amplitude for the dc power supply. Next, the diode rectifier converts the input sinusoid \( v_s \) to a unipolar pulsating waveform output. This pulsating waveform makes it unsuitable as a dc source for electronic circuits, hence the need for a filter. The variations in the magnitude of the rectifier output are considerably reduced by the filter. The output of the rectifier filter still contains a time-component, known as ripple. To reduce the ripple and to stabilized the magnitude of the dc output voltage, a voltage regulator is employed.

![Figure 3.33 Block diagram of a line-operated dc power supply. [6]](image)

3.6 Power Transformers

Basically, a transformer consists of at least two windings, or coils, wrapped around a laminated iron core, see Figure 3.34. A transformer may have multiple secondaries, and one or more of these windings may be center-tapped. Here, the symbols of a normal transformer and a center-tapped transformer are shown in Figure 3.35 (a) and (b), respectively.
Figure 3.34 A transformer with two windings.

Here, the dots are used to indicate the phase of the transformer. When the output waveform is in phase with the input waveform, we can use Figure 3.36 (a) to shows that condition. However, Figure 3.36 (b) is used when the output waveform in 180° out of phase with the input waveform. Moreover, Figure 3.37 shows the how to use 2 dots to indicate the phase of the output waveform for the center-tapped transformer.
In Phase

(b) 180° out of phase

Figure 3.36 the phase of the transformer

(a) Referred to the end of each winding
(b) Referred to the center tap

Figure 3.37 the phase of the center-tapped transformer
If we assume that the transformer is ideal, Relationships between primary and secondary voltages becomes

\[
\frac{V_1}{V_2} = \frac{N_1}{N_2} \quad \text{and} \quad P_{\text{in}} = P_{\text{out}}
\]

where \( \frac{N_1}{N_2} = \text{turn ratio} \)

### 3.7 Rectifiers
A rectifier circuit converts an ac voltage to a pulsating DC voltage. Three types of rectifier circuits are discussed here.

1. (1) Half-wave rectifier
2. (2) Center-tapped full-wave rectifiers
3. (3) Bridge full-wave rectifiers

#### 3.7.1 Half-Wave Rectifiers
Figure 3.38 illustrates the process called half-wave rectification. A diode is connected to an ac source and to a load resistor, \( R_L \), forming a half-wave rectifier. Let’s examine what happens during one cycle of the input voltage using the CVD model for the diode. When the sinusoidal input voltage (\( V_{\text{in}} \)) goes positive, the diode is forward-biased and conducts current through the load resistor, as shown in part (a). The current produces an output voltage across the load \( R_L \), which has the same shape as the positive half-cycle of the input voltage.

When the input voltage goes negative during the second half of its cycle, the diode is reverse-biased. There is no current, so the voltage across the load resistor is 0 V, as shown in Figure 3.38(b). The net result is that only the positive half-cycles of the ac input voltage appear across the load. Since the output does not change polarity, it is a pulsating dc voltage with a frequency of 60 Hz, as shown in part (c).
Figure 3.38 Half-wave rectifier operation. [5]
The comparison between input and output waveform of the half-wave rectifier using CVD diode model is shown in Figure 3.39.

Here, the average value of the half-wave rectified output voltage is the value you would measure on a dc voltmeter. Mathematically, it is determined by

\[ V_{av} = \frac{V_o(p)}{\pi} = \frac{V_p - V_{on}}{\pi} = \frac{V_p - 0.7}{\pi} \]

Then, the average current \( I_D \) through the diode is

\[ I_D = \frac{V_{av}}{R} = I_R \]

**Peak Inverse Voltage (PIV) for Half-Wave Rectifiers**

The maximum amount of reverse bias that a diode will be exposed to in a rectifier is called the **peak inverse voltage or PIV** of the rectifier. From Figure 3.40, for the half-wave rectifier, the value of PIV is found as

\[ PIV = V_p \]
Figure 3.40 PIV occurs at the peak of each negative half-cycle. [6]

Example 8: Find the average value of each half-wave rectified voltage.

(a)

(b)
Solution:

(a) \( V_{av} = \frac{V_{out(p)}}{\pi} = \frac{5}{\pi} \) V

(b) \( V_{av} = 10 + \frac{(20-10)}{\pi} = 10 + \frac{10}{\pi} \) V

(c) \( V_{av} = -15 + \frac{(5-(-15))}{\pi} = -15 + \frac{20}{\pi} \) V
Example 9: Draw the output voltages of each rectifier for the indicated input voltages, as shown in Figure 3.42. The 1N4001 and 1N4003 are specific rectifier diodes.

![Diagram of circuit (a)](image1)

![Diagram of circuit (b)](image2)

**Figure 3.42 For Example 9 [5]**

**Solution:**

The peak output voltage for circuit (a) is

\[ V_{p(out)} = V_{p(in)} - 0.7 \ V = (5 - 0.7) \ V = 4.3 \ V \]

The peak output voltage for circuit (b) is

\[ V_{p(out)} = V_{p(in)} - 0.7 \ V = (100 - 0.7) \ V = 99.3 \ V \]
The output voltage waveforms are shown in Figure 3.43.

![Figure 3.43 For Example 9 [5]](image)

**Example 10:** Draw the output voltage waveform for the circuit and include the voltage.

![Figure 3.44 For Example 10](image)

**Solution:**

For negative cycle:

\[-V_{out} + V_{on} - V_{in} = 0\]

\[V_{out} = -(V_{in} - V_{on})\]

\[V_{out\ (peak)} = - (V_{in(peak)} - 0.7)\]

\[= - (5 - 0.7)\]

\[= - 4.3 \text{ V}\]
Example 11: Consider this circuit, assuming the practical diode model.

(a) Determine the output waveform of the voltage across $R_L$.

(b) Determine the average output voltage across $R_L$.

(c) Determine the average output current through $R_L$.
Solution : (a) $V_{in\,(pri)} = 150 \ V_{rms} = 150 \times \sqrt{2} \\
= 212.13 \ V_{(p)}$

$V_{in\,(sec)} = \frac{1}{4} \times 212.13 \ V_{(p)} \\
= 53.03 \ V_{(p)}$

Figure 3.47 For Example 11

From Figure 3.47,

$V_{total} = V_{in\,(sec)} - 0.7$

$V_{total\,(p)} = V_{in\,(sec)\,(p)} - 0.7 = 53.03 - 0.7 \\
= 52.33 \ V_{(p)}$

Using Voltage divider,

$V_{out} = \frac{10}{10+5} V_{total\,(p)}$

$V_{out\,(p)} = \frac{10}{15} \times 52.33 \\
= 34.9 \ V_{(p)}$

$V_{av} = \frac{V_{out\,(p)}}{\pi} = \frac{34.9}{\pi} = 11.11 \ V$

$I_{av} = \frac{V_{av}}{R_L} = \frac{11.11 \ V}{10 \ \Omega} = 1.111 \ A$
Figure 3.48 For Example 11

Figure 3.49 $V_{out}$ and $V_{in}$ waveform
3.7.2 Center-tapped full-wave rectifiers

A full-wave rectifier allows unidirectional (one-way) current through the load during the entire 360° of the input cycle, whereas a half-wave rectifier allows current through the load only during one-half of the cycle. The result of full-wave rectification is an output voltage with a frequency twice the input frequency and that pulsates every half-cycle of the input, as shown in Figure 3.50.

Figure 3.50 Full-wave rectification. [5]

Here, a center-tapped rectifier is a type of full-wave rectifier that uses two diodes connected to the secondary of a center-tapped transformer, as shown in Figure 3.51. The input voltage is coupled through the transformer to the center-tapped secondary. Half of the total secondary voltage appears between the center tap and each end of the secondary winding as shown.

Figure 3.51 A center-tapped full-wave rectifier. [5]
For a positive half-cycle of the input voltage, the polarities of the secondary voltages are as shown in Figure 3.52(a). This condition forward-biases diode $D_1$ and reverse-biases diode $D_2$. The current path is through $D_1$ and the load resistor $R_L$, as indicated. For a negative half-cycle of the input voltage, the voltage polarities on the secondary are as shown in Figure 3.52(b). This condition reverse-biases $D_1$ and forward-biases $D_2$. The current path is through $D_2$ and $R_L$, as indicated. Because the output current during both the positive and negative portions of the input cycle is in the same direction through the load, the output voltage developed across the load resistor is a full-wave rectified dc voltage, as shown.

Figure 3.52 Basic operation of a center-tapped full-wave rectifier. Note that the current through the load resistor is in the same direction during the entire input cycle, so the output voltage always has the same polarity. [5]
The comparison between input and output waveform of the center-tapped full-wave rectifier using CVD diode model is shown in Figure 3.53.

![Figure 3.53 Input and output waveforms. [6]](image)

The ripple frequency \( f_r(FW) \) is doubled from the line frequency. Therefore,

\[
f_r(FW) = 2f_{line}
\]

The average value \( V_{av} \) of \( V_o \) is

\[
V_{av} = \frac{2V_{O(peak)}}{\pi} = \frac{2(V_p - V_{on})}{\pi}
\]

The average current through load \( R \) is

\[
I_R = \frac{V_{av}}{R}
\]
Since each diode conducts only each half of the cycles, the average current through each diode is

\[ I_D = \frac{I_R}{2} \]

**Peak Inverse Voltage (PIV) for center-tapped full-wave rectifier:**

Each diode in the full-wave rectifier is alternately forward-biased and then reverse-biased. The maximum reverse voltage that each diode must withstand is the peak secondary voltage \( V_{p(\text{sec})} \). This is shown in Figure 3.54 where \( D_2 \) is assumed to be reverse-biased (red) and \( D_1 \) is assumed to be forward-biased (green) to illustrate the concept.

![Diode reverse voltage](image)

Figure 3.54 Diode reverse voltage. [5]

When the total secondary voltage \( V_{\text{sec}} \) has the polarity shown, the maximum anode voltage of \( D_1 \) is \( +\frac{V_{p(\text{sec})}}{2} \) and the maximum anode voltage of \( D_2 \) is \( -\frac{V_{p(\text{sec})}}{2} \). Since \( D_1 \) is assumed to be forward-biased, its cathode is at the same voltage as its anode minus the diode drop; this is also the voltage on the cathode of \( D_2 \).
The peak inverse voltage across D₂ is

\[
\text{PIV} = \left( \frac{V_{p(\text{sec})}}{2} - 0.7 \text{ V} \right) - \left( -\frac{V_{p(\text{sec})}}{2} \right) = \frac{V_{p(\text{sec})}}{2} + \frac{V_{p(\text{sec})}}{2} - 0.7 \text{ V} \\
= V_{p(\text{sec})} - 0.7 \text{ V}
\]

Since \( V_{P(out)} = \frac{V_{P(\text{sec})}}{2} - 0.7 \text{ V} \), then

\[
V_{P(\text{sec})} = 2V_{P(out)} + 1.4 \text{ V}
\]

Therefore, the PIV across either diode in the full-wave center-tapped rectifier is

\[
\text{PIV} = 2V_{P(out)} + 0.7 \text{ V}
\]

**Example 12:**

(a) Show the voltage waveforms across each half of the secondary winding and across \( R_L \) when a 100 V peak sine wave is applied to the primary winding in Figure 3.55.

(b) Calculate the value of PIV of either diode?

![Figure 3.55 For Example 12][5]
Solution:

(a) The transformer turns ratio n = 0.5. The total peak secondary voltage is

\[ V_{p(sec)} = 0.5 \times (100 \text{ V}) = 50 \text{ V} \]

\[ \frac{V_{p(sec)}}{2} = 25 \text{ V} \]

This is a 25 V peak across each half of the secondary with respect to the ground.

\[ V_{out\ (peak)} = \frac{V_{p(sec)}}{2} - V_{on} \]

\[ = 25 - 0.7 = 24.3 \text{ V} \]

The waveforms are shown in Figure 3.56.

![Figure 3.56 output voltage waveforms. [5]](image)

(b) Each diode must have a PIV rating of

\[ \text{PIV} = 2V_{p(out)} + 0.7 \text{ V} = 2(24.3 \text{ V}) + 0.7 \text{ V} = 49.3 \text{ V} \]
**Example 13:** Consider this circuit, assuming the practical diode model.

(a) Determine the output waveform of the voltage across $R_L$.
(b) Determine the average output voltage across $R_L$.
(c) Determine the average output current through $R_L$.

![Circuit Diagram](image)

Figure 3.57 For Example 13.

**Solution:**

(a) For + cycle, $D_1$ = on, $D_2$ = off.

\[-V_s + 0.7 \text{ V} - 10 \text{ V} + V_{out} = 0\]

\[V_{out} = V_s + 10 - 0.7 \text{ V}\]

\[V_{out(p)} = V_p + 10 \text{ V} - 0.7 \text{ V}\]

![Circuit Diagram](image)

Figure 3.58 For Example 13.
Here, 

\[ V_{pri(p)} = 120 \times \sqrt{2} = 169.7 V(p) \]

\[ V_{sec(p)} = \frac{1}{4} \times 169.7 = 42.43 V(p) \]

\[ V_{each(p)} = V_{s(p)} = V_p = \frac{V_{sec(p)}}{2} = 21.21 V(p) \]

\[ V_{out(p)} = V_p + 10 V - 0.7 V \]

\[ = 21.21 + 10 - 0.7 \]

\[ = 30.51 V(p) \]

The output waveform of the voltage across R_L is shown in Figure 3.59.

![Figure 3.59 output waveform of the voltage across R_L](image-url)
3.7.3 Bridge full-wave rectifiers

The bridge rectifier uses four diodes connected as shown in Figure 3.60. When the input cycle is positive as in part (a), diodes $D_1$ and $D_2$ are forward-biased and conduct current in the direction shown. A voltage is developed across $R_L$ that looks like the positive half of the input cycle. During this time, diodes $D_3$ and $D_4$ are reverse-biased.

\[ V_{av} = 10 + \frac{20.51 \times 2}{\pi} = 23.06 \, V \]

\[ I_{av} = \frac{V_{av}}{R_L} = \frac{23.06}{1K\Omega} = 23.06 \, mA \]

Figure 3.60 Operation of a bridge rectifier. [5]
When the input cycle is negative as in Figure 3.60(b), diodes D₃ and D₄ are forward biased and conduct current in the same direction through \( R_L \) as during the positive half-cycle. During the negative half-cycle, D₁ and D₂ are reverse-biased. A full-wave rectified output voltage appears across \( R_L \) as a result of this action.

From Figure 3.61, two diodes are always in series with the load resistor during both the positive and negative half-cycles. If these diode drops are taken into account, the output voltage is

\[
V_{P(out)} = V_{P(sec)} - 1.4 \text{ V}
\]

![Figure 3.61 Bridge operation during a positive half-cycle of the primary and secondary voltages. [5]](image)

The ripple frequency \( f_r(FW) \) is doubled from the line frequency. Therefore,

\[
f_r(FW) = 2f_{line}
\]
The comparison between input and output waveform of the bridge full-wave rectifier using CVD diode model is shown in Figure 3.62.

![Figure 3.62 output waveforms of bridge full wave rectifier. [6]](image)

The average value $V_{av}$ of $V_o$ is

$$V_{av} = \frac{2V_{o(peak)}}{\pi} = \frac{2(V_p - 2V_{on})}{\pi}$$

The average current through load $R$ is

$$I_R = \frac{V_{av}}{R}$$

And the average current through each diode is

$$I_D = \frac{I_R}{2}$$
**Peak Inverse Voltage (PIV) for bridge full-wave rectifier:**

To determine the peak inverse voltage (PIV) of each diode, consider the circuit during the positive half cycles. Apply KVL to the loop formed by D₄, D₂ and R.

\[ V_{D4} + V_{P(\text{sec})} - 2V_{on} + V_{on} = 0 \]

Then,

\[ \text{PIV} = V_{P(\text{sec})} - V_{on} \quad \text{or} \quad \text{PIV} = V_{P(\text{out})} + V_{on} \]

**Example 14:** Determine the peak output voltage for the bridge rectifier in this figure. Assuming the practical model, what PIV rating is required for the diode? The transformer is specified to have a 12 Vrms secondary voltage for the standard 110 V across the primary.

![Figure 3.63 For Example 14. [5]](image)

**Solution:**

\[ V_{P(\text{sec})} = \sqrt{2}V_{rms} = \sqrt{2 \times 12} \approx 17 \text{ V} \]
\[ V_{P(\text{OUT})} = V_{P(\text{sec})} - 2V_{on} = 17 - 1.4 = 15.6 \text{ V} \]
The PIV rating for each diode is

\[ PIV = V_{P(sec)} - V_{on} = 17 - 0.7 = 16.3 \text{ V} \]

or \[ PIV = V_{P(out)} + V_{on} = 15.6 + 0.7 = 16.3 \text{ V} \]

### 3.8 Homework 4

1. Draw the output voltage of each rectifier for the indicated input voltages, as shown in this figure 3.64.

![Figure 3.64](image)

Figure 3.64 For problem 1. [5]
2. Determine the peak value of the output voltage if the turn ratio is 0.5.

3. Consider the circuit in Figure 3.66, assuming the practical diode model.
   (a) Determine the output waveform of the voltage across $R_L$.
   (b) Determine the average output voltage across $R_L$.
   (c) Determine the average output current through $R_L$. 

Figure 3.65 For problem 2. [5]

Figure 3.66 For problem 3. [5]
4. Consider the circuit in Figure 3.67, assuming the practical diode model.

(a) Determine the output waveform of the voltage across $R_L$.

(b) Determine the average output voltage across $R_L$.

(c) Determine the average output current through $R_L$.

5. Consider this circuit, assuming the practical diode model.

(a) What is the total peak secondary voltage?

(b) Find the peak voltage across each half of the secondary.

(c) Sketch the voltage waveform across $R_L$.

(d) What is the PIV for each diode?
6. Consider the circuit in Figure 3.69, assuming the practical diode model.

(a) Determine the average output voltage across \( R_L \).

(b) Sketch the output voltage waveform across \( R_L \).

(c) What is the PIV for each diode?

Figure 3.69 For problem 6.
7. (a) Consider the circuit in Figure 3.70 (a), assuming the practical diode model. Sketch the output voltage waveform across $R_L$. Assume $V_{on} = 0.7$ V for each diode.

(b) Consider the circuit in Figure 3.70 (b), assuming the practical diode model. Sketch the output voltage waveform across $R_L$. Assume $V_{on} = 0.7$ V for each diode.

Figure 3.70 For problem 7.
8. (a) Consider the circuit in Figure 3.71(a), assuming the CVD model. Sketch the output voltage waveform across 10 Ω resistor, and then find the average voltage ($V_{av}$). Assume $V_{on} = 0.7$ V for each diode.

(b) Consider the circuit in Figure 3.71(b), assuming the CVD model. Sketch the output voltage waveform across 10 Ω resistor, and then find the average voltage ($V_{av}$). Assume $V_{on} = 0.7$ V for each diode.

Figure 3.71 For problem 8.
9. Consider the Center-tapped full wave rectifier circuits in Figure 3.72 (a) and that in Figure 3.72 (b), then sketch the output waveform of the voltage across $R_L (V_{OUT})$ in both circuits.

(a)

(b)

Figure 3.72 For problem 9.
10. Determine the peak output voltage for the bridge rectifier in this figure. Assuming the practical model, what PIV rating is required for the diode? Assume that the primary voltage of the transformer is 200 V\(_{p-p}\) and the transformer turns ratio \(n = 0.25\).

![Figure 3.73 For problem 10. [5]](image)

11. Using practical diode model, find the output voltage across \(R_L\), PIV of each diode and plot the output waveform of output voltage across \(R_L\).

\[
10 : 1
\]

![Figure 3.74 For problem 11.](image)
12. (a) Sketch the output voltage of the bridge rectifier in Figure 3.75. Notice that all the Si diodes are reversed from the normal full-wave bridge rectifier circuits.

(b) Determine the average output voltage ($V_{av}$) across $R_L$.

![Figure 3.75 For problem 12. [5]](image)

13. Consider the circuit in figure 3.76,

(a) Sketch the output waveform of the voltage across $R_L$ ($V_{OUT}$)

(b) Determine the average output voltage across $R_L$ ($V_{AV}$)

(c) Determine the average output current through $R_L$

![Figure 3.76 For problem 13.](image)
3.9 Capacitive Filters [5], [6]

In most power supply applications, AC power line must be converted to an approximately constant DC voltage. The pulsating DC output of a half-wave rectifier or that of a full-wave rectifier must be filtered to reduce the large voltage variations. Figure 3.77 illustrates the filtering concept showing a nearly smooth DC output voltage from the filter. The small amount of fluctuation in the filter output voltage is called ripple.

![Diagram of full-wave rectifier and filter](image)

(a) Rectifier without a filter

(b) Rectifier with a filter (output ripple is exaggerated)

Figure 3.77 Power supply filtering. [5]

A half-wave rectifier with a capacitor-input filter is shown in Figure 3.78. Figure 3.78 (a) shows that during the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7 V of the input peak. When the input begins to decrease below its peak, as illustrated in part (b), the capacitor retains its charge and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only through the load resistance at a rate determined by the $R_LC$ time constant. The larger the time constant, the less capacitor will discharge.
During the first quarter of the next cycle, as illustrated in Figure 3.78 (c), the diode will again become forward-biased when the input voltage exceeds the capacitor voltage by 0.7 V.

Figure 3.78 Operation of a half-wave rectifier with a capacitor-input filter. The current indicates charging or discharging of the capacitor. [5]
Ripple Voltage:

As you have seen, the capacitor quickly charges at the beginning of a cycle and slowly discharges through $R_L$ after the positive peak of the input voltage (when the diode is reverse-biased). The variation in the capacitor voltage due to the charging and discharging is called the *ripple voltage*. Generally, ripple is undesirable; thus, the smaller the ripple, the better the filtering action, as illustrated in Figure 3.79.

For a given input frequency, the output frequency of a full-wave rectifier is twice that of a half-wave rectifier, as illustrated in Figure 3.80. This makes a full-wave rectifier easier to filter because of the shorter time between peaks. When filtered, the full-wave rectified voltage has a smaller ripple than does a half-wave voltage for the same load resistance and capacitor values. The capacitor discharges less during the shorter interval between full-wave pulses, as shown in Figure 3.81.
Ripple Factor:

The ripple factor \( r \) is an indication of the effectiveness of the filter and is defined as

\[
   r = \frac{V_{r(pp)}}{V_{DC}}
\]

\( r \) = Ripple Factor
\( V_{r(pp)} \) = peak – to – peak ripple voltage
\( V_{DC} \) = DC (average) Voltage of the filter’s output voltage

Here,

\[
   V_{DC} \approx \left(1 - \frac{1}{2fR_LC}\right)V_{p(rect)}
\]

\[
   V_{r(pp)} = \left(\frac{1}{fR_LC}\right)V_{p(rect)}
\]
From Figure 3.82, $V_{r(pp)}$ is the peak-to-peak ripple voltage and $V_{DC}$ is the dc (average) value of the filter’s output voltage. The lower the ripple factor, the better the filter. The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load resistance.

Example 15: Determine the ripple factor for the filtered bridge rectifier with a load as indicated in Figure 3.83.
Solution:

\[ V_{F(\text{pri})} = \sqrt{2} V_{\text{rms(pri)}} = \sqrt{2} \times 115 \approx 163 \text{ V} \]

\[ V_{F(\text{sec})} = \frac{n_2}{n_1} \times V_{F(\text{pri})} = \frac{1}{60} \times V_{F(\text{pri})} = \frac{1}{60} \times 163 = 16.3 \text{ V} \]

\[ V_M = V_{F(\text{sec})} - 2V_{\text{on}} = 16.3 - 1.4 = 14.9 \text{ V} \]

For full-wave rectifier:

\[ f_r = 2f_{\text{line}} = 2 \times 60 = 120 \text{ Hz} \]

\[ V_r = \frac{V_M}{R_L f_r C} = \frac{14.9}{2.2 \text{ k}\Omega \times 120 \text{ Hz} \times 50 \mu\text{F}} = 1.13 \text{ V} \]

\[ V_{DC} = V_M - \frac{V_r}{2} = V_{F(\text{sec})} - 2V_{\text{on}} - \frac{V_r}{2} = 16.3 - 1.4 - \frac{1.13}{2} = 14.3 \text{ V} \]

or

\[ V_{DC} = V_M \left(1 - \frac{1}{2 f_r RC}\right) = 14.9 \times \left(1 - \frac{1}{(240 \text{ Hz})(2.2 \text{ k}\Omega)(50 \mu\text{F})}\right) = 14.3 \text{ V} \]

ripple factor \( r = \frac{V_{r(F-F)}}{V_{DC}} = \frac{1.13}{14.3} = 0.079 \)

Example 16:

Consider the filtered half-wave rectifier in Figure 3.84. Assume \( f_{\text{line}} = 60 \text{ Hz} \) and \( V_{\text{on}} = 0.7 \text{ V} \). Given the following conditions:

(1) \( V_{DC} = 15 \text{ V} \) when \( R_L = 1 \text{ k}\Omega \)

(2) \( V_{DC} = 20 \text{ V} \) when \( R_L = 1.5 \text{ k}\Omega \)
Determine

(a) Filter capacity (C)

(b) Maximum ripple voltage ($V_{p(rect)}$ or $V_M$)

(c) Turn ratio ($N_1 : N_2$)

![Diagram of filter circuit with transformer and capacitor](image)

Figure 3.84 For Example 16

Solution:

(a) For the half-wave rectifier; $f_r = f_{line} = 60$ Hz

Here, (1) $V_{DC} = 15$ V when $R_L = 1$ kΩ

(2) $V_{DC} = 20$ V when $R_L = 1.5$ kΩ

$$V_{DC} = V_M \left( 1 - \frac{1}{2f_rRC} \right)$$

$$\therefore \quad 15 = V_M \times \left( 1 - \frac{1}{(2 \times 60 \text{ Hz})(1 \times 10^{-3} \Omega)(C)} \right) \quad (1)$$

$$20 = V_M \times \left( 1 - \frac{1}{(2 \times 60 \text{ Hz})(1.5 \times 10^{-3} \Omega)(C)} \right) \quad (2)$$

From (1) and (2):

$$C = 1.67 \times 10^{-5} \text{ F} \quad \text{or} \quad 16.7 \mu\text{F}$$
(b) 

\[ 15 = V_M \times \left( 1 - \frac{1}{(2 \times 60 \text{ Hz})(1 \times 10^{-3} \Omega)(1.67 \times 10^{-5} \text{ F})} \right) \]

\[ \therefore V_M \cong 30 \text{ V} \]

(c) From Figure 3.85,

\[ V_{\text{sec}(p)} - 0.7 = V_M \]

\[ \therefore V_M = 30.7 \text{ V} \]

\[ V_{\text{pri}(p)} = \sqrt{2} \times 125 = 176.78 \text{ V(p)} \]

\[ \therefore \frac{N_1}{N_2} = \frac{V_{\text{pri}(p)}}{V_{\text{sec}(p)}} = \frac{176.78}{30.7} = 5.76 \]

Figure 3.85 For Example 16.
3.10 Voltage Regulators [5], [6]

The use of a filter will greatly reduce the variations in the output from a rectifier. At the same time, the ideal power supply would provide a stable dc output voltage that had no ripple voltage at all. While there will always be some ripple voltage at the output, the use of a voltage regulator will reduce the filter output ripple. The primary function of the voltage regulator is to maintain a constant DC output voltage by rejecting any ripple voltage that is not removed by a filter. Here, the simplest voltage regulator is the Zener diode. However, better regulation can be obtained with integrated circuits that are specially designed for this purpose.

3.10.1 Percent of Voltage Regulation (% VR)

Ideally, a voltage regulator should keep the output voltage constant for all values of load current. However, in general the output or load voltage ($V_o$ or $V_L$) will tend to decrease as the load current ($I_L$) increases as illustrated below. When the load current is zero (or no load or $I_L = I_{NL}$), the output voltage will be at its maximum value ($V_L = V_{NL}$). When the load current is maximum ($I_L = I_{FL}$), its output voltage is at its minimum value ($V_L = V_{FL}$).

![Diagram showing the relation between load current and load voltage of normal voltage regulator.](image)

**Figure 3.86** Relation between load current and load voltage of normal voltage regulator. [6]
Here, the percent of voltage regulation (% VR) is given as

\[
% \text{ VR} = \left( \frac{V_{NL} - V_{FL}}{V_{FL}} \right) \times 100\%
\]

### 3.10.2 Zener Diodes

The Zener diode is a silicon pn junction device that differs from rectifier diodes because it is designed for operation in the reverse-breakdown region. The V-I characteristics of the Zener diode is shown in Figure 3.87. When a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically. If a Zener diode is forward-biased, it operates the same as a rectifier diode. Moreover the symbol of zener diode is shown in Figure 3.88.

![Figure 3.87 V-I characteristics of Zener diode](image)

Figure 3.87 V-I characteristics of Zener diode [5]

![Figure 3.88 Symbol for the zener diode](image)

Figure 3.88 Symbol for the zener diode.
3.10.3 Zener Regulation

The reverse portion of a zener diode’s characteristics curve is shown in Figure 3.89. Notice that as the reverse voltage ($V_R$) is increased, the reverse current ($I_R$) or zener current ($I_Z$) remains extremely small up to the “knee” of the curve. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance ($Z_Z$), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the zener breakdown voltage ($V_Z$) remains essentially constant although it increases slightly as the zener current ($I_Z$) increases. Under this condition, we can calculate the zener impedance ($Z_Z$) by

\[ Z_Z = \frac{\Delta V_Z}{\Delta I_Z} \]

![Figure 3.89 Breakdown Characteristics of Zener diode. [5]]
A minimum value of reverse current, $I_{ZK}$, must be maintained in order to keep the diode in breakdown of voltage regulation. Also, there is a maximum current, $I_{ZM}$, above which the diode maybe damaged due to excessive power dissipation. Therefore, the zener diode maintains a nearly constant voltage across its terminal for values of reverse current ranging from $I_{ZK}$ to $I_{ZM}$. Moreover, a nominal zener voltage, $V_{ZT}$, is usually specified on a data sheet at a value of reverse current called the zener test current, $I_{ZT}$.

**Zener Regulation with a Varying Input Voltage:**

Figure 3.90 illustrates how a zener diode can be used to regulate a varying dc voltage. As the input voltage varies (within limits), the zener diode maintains a nearly constant output voltage across its terminals. However, as $V_{IN}$ changes, $I_Z$ will change proportionally so that the limitations on the input voltage variation are set by the minimum and maximum current values ($I_{ZK}$ and $I_{ZM}$) with which the zener can operate.

![Figure 3.90](image)

(a) As the input voltage increases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

(b) As the input voltage decreases, the output voltage remains constant ($I_{ZK} < I_Z < I_{ZM}$).

Figure 3.90 Zener regulation with a varying input voltage [5]
Zener Regulation with a Variable Load (from no load to full load):

Figure 3.91 shows a zener voltage regulator with a variable load resistor across the terminals. The zener diode maintains a nearly constant voltage across RL as long as the zener current is greater than $I_{ZK}$ and less than $I_{ZM}$.

![Zener Regulation Diagram](image)

Figure 3.91 Zener regulation with a variable load [5]

When the output terminals of the zener regulator are open ($R_L = \infty$), the load current is zero and all of the current is through the zener. When a load resistor $R_L$ is connected, part of the total current is through the zener and part through $R_L$. As $R_L$ is decreased, the load current $I_L$ increases and $I_Z$ decreases. The zener diode continues to regulate the voltage until $I_Z$ reaches its minimum value, $I_{ZK}$. At this point the load current is maximum. The total current through $R$ remains essentially constant.

3.10.4 Zener Reduction of Ripple Voltage

The zener regulation can reduce the amount of ripple voltage present at the filter output. The basic zener regulator and its equivalent circuit are shown in Figure 3.92. To the ripple waveform, there is a voltage divider present in the regulator. This voltage divider is made up of the series resistance ($R_s$) and the parallel combination of $Z_Z$ and the load.
The ripple output from the regulator can be found as

\[ V_{r(out)} = \frac{(Z_Z // R_L)}{(Z_Z // R_L) + R_S} V_r \]

**Example 17:** Determine the minimum and the maximum load currents for which the zener diode will maintain regulation. What is the minimum value of \( R_L \) that can be used? \( V_Z = 12 \) V, \( I_{ZK} = 1 \) mA, and \( I_{ZM} = 50 \) mA. Assume \( Z_Z = 0 \) \( \Omega \) and \( V_Z \) remains a constant 12 V over the range of current values, for simplicity.

![Figure 3.93 For Example 17. [5]](image-url)
Solution:

Using KCL, we get

\[ I_T = I_Z + I_L \]

\[ \therefore I_L = I_T - I_Z \]

\[ I_{L_{\text{max}}} = I_T - I_{Z_{\text{min}}} = I_T - I_{Z_{K}} \]

When \( I_L = 0 \) A (\( R_L = \infty \) \( \Omega \)), \( I_Z \) is maximum and equal to the total circuit \( I_T \).

\[ I_{Z_{\text{max}}} = I_T = \frac{V_{\text{in}} - V_Z}{R} = \frac{24 - 12}{470} = 25.5 \text{ mA} \]

Since \( I_{Z_{\text{max}}} < I_{Z_{M}} \), 0 A is an acceptable minimum value of \( I_L \) because the Zener can handle all of the 25.5 mA

\[ \therefore I_{L_{\text{min}}} = 0 \text{ A} \]

The maximum value of \( I_L \) occurs when \( I_Z \) is minimum (\( I_Z = I_{Z_K} \)), so solve for \( I_{L_{\text{max}}} \):

\[ I_{L_{\text{max}}} = I_T - I_{Z_K} = 25.5 \text{ mA} - 1 \text{ mA} = 24.5 \text{ mA} \]

The minimum value of \( R_L \) is

\[ R_{L_{\text{min}}} = \frac{V_Z}{I_{L_{\text{max}}}} = \frac{12 \text{ V}}{24.5 \text{ mA}} = 490 \text{ } \Omega \]

*** Notice that if \( R_L \) is less than 490 \( \Omega \), \( R_L \) will make more current away from the zener diode and \( I_Z \) will be reduced below \( I_{Z_K} \). This will cause the zener to lose regulation.***
3.10.5 Terminal Voltage Regulator ICs

The most popular IC regulators have three terminals- an input terminal, an output terminal, and a reference terminal. From Figure 3.94 (a), three-terminal regulators designed for a fixed output voltage require only external capacitor to complete the regulation portion of the power supply. Filtering is accomplished by a large-value capacitor between the input voltage and ground. Finally, an output capacitor (typically 0.1 μF to 1.0 μF) is placed in parallel with the output to improve the transient response.

![Diagram](image)

(a) Standard configuration

<table>
<thead>
<tr>
<th>Type number</th>
<th>Output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>7805</td>
<td>+5.0 V</td>
</tr>
<tr>
<td>7806</td>
<td>+6.0 V</td>
</tr>
<tr>
<td>7808</td>
<td>+8.0 V</td>
</tr>
<tr>
<td>7809</td>
<td>+9.0 V</td>
</tr>
<tr>
<td>7812</td>
<td>+12.0 V</td>
</tr>
<tr>
<td>7815</td>
<td>+15.0 V</td>
</tr>
<tr>
<td>7818</td>
<td>+18.0 V</td>
</tr>
<tr>
<td>7824</td>
<td>+24.0 V</td>
</tr>
</tbody>
</table>

(b) The 7800 series

Figure 3.94 Configuration and type number of standard IC regulator. [5]

Examples of fixed three-terminal regulators are the 78XX series of regulators that are available with various output voltages and can supply up to 1 A of load current. From Figure 3.94 (b), the last two digits of the number stand for the output voltage; thus, the 7812 has +12 V output. The LM78XX series offer
output voltages of 5, 6, 8, 9, 12, 15, 18 and 24 V. Similarly, the LM79XX series has output voltages of -5, -6, -8, -9, -12, -15, -18 and -24 V. Here, a basic fixed +5 V power supply with a 7805 regulator is shown in Figure 3.95.

Figure 3.95 A basic +5.0 V regulated power supply. [5]

3.11 Putting It All Together [2], [5], [6]

Figure 3.96 Configuration of line-operated DC power supply. [2]
We have discussed the operation of transformers, rectifiers, filters, and zener regulators in detail. Now, it is time to put them all together into a basic working power supply. The DC power supply shown in Figure 3.96 contains a transformer, bridge rectifier, capacitive filter, and zener diode voltage regulator.

The transformer converts the incoming line voltage to a lower secondary voltage. The bridge rectifier converts the transformer secondary AC voltage into a positive pulsating DC voltage. This pulsating DC voltage is applied to the capacitive filter, which reduces the variations in the rectifier DC output voltage. Finally, the zener voltage regulator is used to keep the DC output voltage from the power supply remain relatively constant.

**Example 18:** Determine the values of $V_{DC}$, $V_{r(out)}$, and $I_L$ for the power supply shown in Figure 3.97.

![Figure 3.97 For Example 18. [2]](image_url)
Solution:

The dc output voltage ($V_{DC}$) will equal the value of $V_Z$, by formula:

$$V_{DC} = V_Z = 30 \text{ V}$$

And

$$I_L = \frac{V_{dc}}{R_L} = \frac{30 \text{ V}}{300 \Omega} = 100 \text{ mA}$$

To find $V_{r(out)}$, it is found that

$$V_{P(sec)} = 36 \times 1.414 \approx 51 V_{(P)}$$

$$V_M = V_{P(sec)} - 2V_{on} = 51 - 1.4 = 49.6 V_{(P)}$$

Here,

$$I_{Rs} = \frac{V_M - V_S}{R_S} = \frac{49.6 - 30}{75} = 0.26133 \text{ A} = 261.33 \text{ mA}$$

$$V_r \approx \frac{I_{Rs}}{f_C} = \frac{0.26133}{(2 \times 60)(2200 \times 10^{-6})} = 989.77 \text{ mV}_{(p-p)}$$

Finally, the value of $V_{r(out)}$ is found as

$$V_{r(out)} = \frac{(Z_Z // R_L)}{(Z_Z // R_I) + R_S} V_r = \frac{(60//300)}{(60//300)+75} 989.77 \text{ mV}_{(p-p)}$$

$$\approx 396 \text{ mV}_{(p-p)}$$
Example 19:

(a) Determine the values of $V_{DC}$, $V_{r(out)}$, and $I_L$ for the power supply shown in Figure 3.98.

(b) Can we use the zener diode in this circuit as the voltage regulator or not? Why?

Solution:

(a)

$$V_{dc} = V_Z = 10\, \text{V}, \quad I_L(\text{or} I_{DC}) = \frac{V_{dc}}{R_L} = \frac{10\, \text{V}}{1000\, \Omega} = 10\, \text{mA}$$

$$V_{F(\text{primary})} = \frac{250\, \text{V(p - p)}}{2} = 125\, \text{V(p)}$$

$$V_{F(\text{secondary})} = \frac{1}{4} \times V_{F(\text{primary})} = \frac{1}{4} \times 125 = 31.5\, \text{V(p)}$$
\[ V_M = V_{P(\text{secondary})} - 0.7 = 31.25 - 0.7 = 30.55 \text{ V(p)} \]

\[ I_{R_S} = \frac{V_M - V_S}{R_S} = \frac{30.55 - 10}{100} = 0.2055 \text{ A} = 205.5 \text{ mA} \]

\[ V_r \equiv \frac{I_{R_S}}{f_r C}, f_r = f_{\text{line}} = 60 \text{Hz} \quad \text{ (half-wave rectifier)} \]

\[ = \frac{0.2055}{(60)(2500 \times 10^{-6})} = 1.37 \text{ V(p-p)} \]

\[ V_{r(\text{cur})} = \frac{(Z_Z // R_L)}{(Z_Z // R_L) + R_S} V_r = \frac{(50 // 100)}{(50 // 100) + 100} 1.37 \text{ V(p-p)} \]

\[ \equiv 442 \text{ mV(p-p)} \]

(b) \[ I_{RS} = I_Z + I_L \]

Here \[ I_Z = I_{RS} - I_L = 205.5 - 10 = 195.5 \text{ mA} \]

*** As \[ I_Z < I_{ZM} \] (195.5 mA < 300 mA), we can use this zener diode as the voltage regulator ***

### 3.12 Homework 5

1. Consider the filtered full-wave rectifier. Assume \[ f_{\text{line}} = 60 \text{ Hz} \] and \[ V_{\text{on}} = 0.7 \text{ V} \].

Given the following conditions:

(1) \[ V_{DC} = 10 \text{ V} \] when \[ R_L = 500 \Omega \]

(2) \[ V_{DC} = 12 \text{ V} \] when \[ R_L = 1500 \Omega \]
Determine

(a) Filter capacity (C)

(b) Maximum ripple voltage ($V_{p(rect)}$ or $V_M$)

Figure 3.99 For problem 1. [5]

2. Calculate the dc output voltage ($V_{DC}$), dc output current ($I_{DC}$) values and the output ripple voltage ($V_{r(out)}$).

Figure 3.100 For problem 2.
3. Calculate the dc output voltage ($V_{DC}$), dc output current ($I_{DC}$) values and the output ripple voltage ($V_{r(out)}$).

![Diagram of a circuit with a transformer, diodes, and filters.]

Figure 3.101 For problem 3.

4. (a) From the circuit of Figure 3.102, Find the values of $V_{DC}$, $I_L$ and $V_{r(out)}$.

(b) Can we use this type of zener diode as the voltage regulator in this circuit? Why?

![Diagram of a different circuit with a transformer, zener diode, and filters.]

Figure 3.102 For problem 4.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_Z$</td>
<td>20 V</td>
</tr>
<tr>
<td>$I_{ZM}$</td>
<td>250 mA</td>
</tr>
</tbody>
</table>
5. Consider the line–operated DC power supply circuit shown in Figure 3.103. Assume $V_{r(out)}$ at $R_L = 0.229 \, V_{(p-p)}$, determine the turn ration $N_1:N_2$ in this circuit.

![Figure 3.103 For problem 5.](image)

6. (a) Determine the values of $V_{DC}$, $V_{r(out)}$, and $I_L$ for the power supply shown in Figure 3.103.

   (b) Can we use the zener diode in this circuit as the voltage regulator or not? Why?

![Figure 3.104 For problem 6.](image)
3.13 Diode Limiter [5]

Diode circuits, called limiters or clippers, are sometimes used to clip off portions of signal voltages above or below certain levels. Figure 3.105(a) shows a diode positive limiter (also called clipper) that limits or clips the positive part of the input voltage. As the input voltage goes positive, the diode becomes forward biased and conducts current. Point A is limited to +0.7 V when the input voltage exceeds this value. When the input voltage goes back below 0.7 V, the diode is reverse-biased and appears as an open. The output voltage looks like the negative part of the input voltage, but with a magnitude determined by the voltage divider formed by $R_1$ and the load resistor, $R_L$, as follows:

$$V_{out} = \left( \frac{R_L}{R_1 + R_L} \right) V_{in}$$

(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V) and reverse-biased during the negative alternation.

(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below −0.7 V) and reverse-biased during the positive alternation.

Figure 3.105 Examples of diode limiters (clippers). [5]
If the diode is turned around, as in Figure 3.105(b), the negative part of the input voltage is clipped off. When the diode is forward-biased during the negative part of the input voltage, point A is held at \(-0.7\) V by the diode drop. When the input voltage goes above \(-0.7\) V, the diode is no longer forward-biased; and a voltage appears across \(R_L\) proportional to the input voltage.

**Example 20:** What would you expect to see displayed on an oscilloscope connected across \(R_L\) in the limiter shown in Figure 3.106?

![Figure 3.106 For Example 20. [5]](image)

**Solution:**

The diode is forward-biased and conducts when the input voltage goes below \(-0.7\) V. So, for the negative limiter, determine the peak output voltage across \(R_L\) by the following equation:

\[
V_{out} = \frac{R_L}{R_1 + R_L} V_{in} = \left(\frac{1\,\text{k}\Omega}{1.1\,\text{k}\Omega}\right) \times 10\,\text{V} = 9.09\,\text{V}
\]
The output waveform is shown as:

![Figure 3.107 Output voltage waveform for Figure 3.106. [5]](image)

**Biased Limiters:**

The level to which an AC voltage is limited can be adjusted by adding a bias voltage, $V_{BIAS}$, in series with the diode, as shown in Figure 3.108. The voltage at point A must equal $V_{BIAS} + 0.7$ V before the diode will become forward-biased and conduct. Once the diode begins to conduct, the voltage at point A is limited to $V_{BIAS} + 0.7$ V so that all input voltage above this level is clipped off.

![Figure 3.108 A positive limiter. [5]](image)
To limit a voltage to a specified negative level, the diode and bias voltage must be connected as in Figure 3.109. In this case, the voltage at point A must go below $-V_{BIAS} - 0.7$ V to forward-bias the diode and initiate limiting action as shown.

Example 21: Figure 3.110 shows a circuit combining a positive limiter with a negative limiter. Determine the output voltage waveform.
Solution:

When the voltage at point A reaches +5.7 V, diode D₁ conducts and limits the waveform to +5.7 V. Diode D₂ does not conduct until the voltage reaches –5.7 V. Therefore, positive voltages above +5.7 V and negative voltages below –5.7 V are clipped off. The resulting output voltage waveform is

![Output voltage waveform](image)

Figure 3.111 Output voltage waveform for Figure 3.110. [5]

### 3.14 Homework 6

1. Draw the voltage waveform of V<sub>OUT</sub> and V<sub>10Ω</sub> in this circuit. Assume D₁ and D₂ are Si diode.

![Circuit diagram](image)

Figure 3.112 For problem 1. [5]
2. Sketch the output waveforms of $V_{OUT1}$, $V_{OUT2}$. And determine the minimum and maximum voltage of both waveforms.

![Output waveforms of $V_{OUT1}$ and $V_{OUT2}$ for problem 2.](image)

Figure 3.113 For problem 2.

3. Sketch the output waveforms of $V_{OUT1}$, $V_{OUT2}$. And determine the minimum and maximum voltage of both waveforms.

![Output waveforms of $V_{OUT1}$ and $V_{OUT2}$ for problem 3.](image)

Figure 3.114 For problem 3.
4. Determine the output waveform for the circuit in Figure 3.115(a) for each input voltage in (b), (c), and (d).

Figure 3.115 For problem 4. [5]
5. Determine the $R_L$ voltage waveform for each circuit in Figure 3.116(a), (b) and (c).

![Figure 3.116 For problem 5. [5]](image)

6. Draw the output voltage waveform for each circuit in Figure 3.117(a) and (b).

![Figure 3.117 For problem 6. [5]](image)
7. Sketch the output waveforms of $V_{OUT\,1}$, $V_{OUT\,2}$, and $V_{OUT\,3}$ in this circuit shown in Figure 3.118. And also determine $V_{\text{max}}$ and $V_{\text{min}}$ of each voltage waveform. Assuming CVD model, and $D_1$ and $D_2$ are Si diodes.

Figure 3.118 For problem 7.